



# The 5th International Workshop on embedded computer Systems: Architectures, MOdeling, and Simulation (SAMOS V)

*July 18-20 2005, Samos, Greece*

## Monday, July 18

### 8:30 **Opening**

*Stamatis Vassiliadis (Delft University of Technology, The Netherlands)*

### Keynote

*Session chair: Stamatis Vassiliadis*

### 8:45 "Platform Thinking in Embedded Systems"

*Bob Iannucci (Nokia, Finland)*

### Reconfigurable Computing

*Session chair: Jarmo Takala*

### 9:30 **Posters**

"Fast Real-Time Job Selection with Resource Constraints under Earliest Deadline First"  
*Sangchul Han (Seoul National University, Korea), Moonju Park (LG Electronics, Korea), and Yookun Cho (Seoul National University, Korea)*

"A Novel JAVA Processor for Embedded Devices"

*Yiyu Tan, Chihang Yau, Kaiman Lo, Paklun Mok, and Anthony S. Fong (City University of Hong Kong, Hong Kong)*

"Formal Specification of a Protocol Processor"

*Tomi Westerlund and Juha Plosila (University of Turku, Finland)*

### 9:50 "Interprocedural Optimization for Dynamic Hardware Configurations"

*Elena Moscu Panainte, Koen Bertels, and Stamatis Vassiliadis (Delft University of Technology, The Netherlands)*

### 10:10 "Reconfigurable Embedded Systems: An Application-Oriented Perspective on Architectures and Design Techniques"

*M. Glesner, H. Hinkelmann, T. Hollstein, L.S. Indrusiak, T. Murgan, A.M. Obeid, M. Petrov, T. Pionteck, and P. Zipf (Darmstadt Univ. Tech., Germany)*

### 10:30 "Reconfigurable Multiple Operation Array"

*Humberto Calderon and Stamatis Vassiliadis (TU Delft, The Netherlands)*

### 10:50 "Data-Driven Regular Reconfigurable Arrays: Design Space Exploration and Mapping"

*Ricardo Ferreira (Universidade Federal de Viçosa, Brazil), João M.P. Cardoso (Universidade do Algarve, Portugal), Andre Toledo (Universidade Federal de Viçosa, Brazil), and Horácio C. Neto (INESC-ID, Portugal)*

*Session chair: Andy Pimentel*

### 11:10 **Posters**

"Flux Caches: What Are They and Are They Useful?"

*Georgi N. Gaydadjiev and Stamatis Vassiliadis (TU Delft, The Netherlands)*

"First-Level Instruction Cache Design for Reducing Dynamic Energy Consumption"  
*Cheol Hong Kim (Seoul National Univ., Korea), Sunghoon Shim (Seoul National Univ., Korea), Jong Wook Kwak (Seoul National Univ., Korea), Sung Woo Chung (Samsung, Korea), and Chu Shik Jhon (Seoul National Univ., Korea)*

"Tuning a Protocol Processor Architecture Towards DSP Operations"  
*Jani Paakkulainen, Seppo Virtanen, and Jouni Isoaho (University of Turku, Finland)*

- 11:30 "Two-Dimensional Fast Cosine Transform for Vector-STA Architectures"  
*J.P. Robelly, A. Lehmann, and G. Fettweis (Technische Universität Dresden, Germany)*
- 11:50 "DDM-CMP: Data-Driven Multithreading on a Chip Multiprocessor"  
*Kyriakos Stavrou, Paraskevas Evripidou, and Pedro Trancoso (University of Cyprus, Cyprus)*
- 12:10 "Observations on Power-Efficiency Trends in Mobile Communication Devices"  
*Olli Silvén (Univ. Oulu, Finland) and Kari Jyrkkä (Nokia, Finland)*
- 12:30 "Hardware Cost Estimation for Application-Specific Processor Design"  
*Teemu Pitkänen, Tommi Rantanen, Andrea Cilio, and Jarmo Takala (Tampere Univ. Tech., Finland)*

## Tuesday, July 19

### Processor Architectures, Design, and Simulation

*Session chair: John Glossner*

- 8:30 "Automatic FIR Filter Generation for FPGAs"  
*Holger Ruckdeschel, Hritam Dutta, Frank Hannig, and Jürgen Teich (University of Erlangen-Nuremberg, Germany)*
- 8:50 "Power-Aware Branch Logic: A Hardware Based Technique for Filtering Access to Branch Logic"  
*Sunghoon Shim (Seoul National Univ., Korea), Jong Wook Kwak (Seoul National Univ., Korea), Cheol Hong Kim (Seoul National Univ., Korea), Sung Tae Jhang (Univ. Suwon, Korea), and Chu Shik Jhon (Seoul National Univ., Korea)*
- 9:10 "Exploiting Intra-Function Correlation with the Global History Stack"  
*Fei Gao and Suleyman Sair (NC State University, USA)*
- 9:30 "Power Efficient Instruction Caches for Embedded Systems"  
*Dinesh C. Suresh, Walid A. Najjar, and Jun Yang (Univ. California, Riverside, USA)*
- 9:50 **Posters**
- "Automatic ADL-Based Assembler Generation for ASIP Programming Support"  
*Leonardo Taglietti, Jose O. Carlomagno Filho, Daniel C. Casarotto, Olinto J.V. Furtado, and Luiz C.V. dos Santos (Federal University of Santa Catarina, Brazil)*
- "A Hardware Accelerator for Controlling Access to Multiple-Unit Resources in Safety/Time-Critical Systems"  
*Philippe Marchand (Concordia University, Canada) and Purnendu Sinha (Indian Institute of Information Technology, India)*
- "Pattern Matching Acceleration for Network Intrusion Detection Systems"  
*Sunil Kim (Hongik University, Korea)*

*Session chair: Georgi Gaydadjiev*

- 10:10 "Micro-Architecture Performance Estimation by Formula"  
*Lucanus J. Simonson (Intel, USA) and Lei He (Univ. California, Los Angeles, USA)*
- 10:30 "Offline Phase Analysis and Optimization for Multi-Configuration Processors"  
*Frederik Vandeputte, Lieven Eeckhout, and Koen De Bosschere (Ghent University, Belgium)*

- 10:50 "CORDIC-Augmented Sandbridge Processor for Channel Equalization"  
*Mihai Sima (Univ. Victoria, Canada), John Glossner (Sandbridge Tech., USA), Daniel Iancu (Sandbridge Tech., USA), Hua Ye (Sandbridge Tech., USA), Andrei Iancu (Rochester Inst. Tech., USA), and A. Joseph Hoane, Jr. (Sandbridge Tech., USA)*
- 11:10 "Ultra Fast Cycle-Accurate Compiled Emulation of Inorder Pipelined Architectures"  
*Stefan Farfeleder (TU Wien, Austria), Andreas Krall (TU Wien, Austria), and Nigel Horspool (University of Victoria, Canada)*
- 11:30 **Posters**
- "Real-Time Stereo Vision on a Reconfigurable System"  
*SungHwan Lee, Jongsu Yi, and JunSeong Kim (Chung-Ang University, Korea)*
- "Application of Very Fast Simulated Reannealing (VFSR) to Low Power Design"  
*Ali Manzak and Huseyin Goksu (Suleyman Demirel University, Turkey)*
- "Compressed Swapping for NAND Flash Memory Based Embedded Systems"  
*Sangduck Park, Hyunjin Lim, Hoseok Chang, and Wonyong Sung (Seoul National University, Korea)*
- Session chair: Wayne Luk*
- 11:50 "Generating Stream Based Code from Plain C"  
*Marcel Beemster, Hans van Someren, Liam Fitzpatrick, and Ruben van Royen (ACE, The Netherlands)*
- 12:10 "A Scalable Embedded JPEG2000 Architecture"  
*Chunhui Zhang, Yun Long, and Fadi Kurdahi (University of California, Irvine, USA)*
- 12:30 "A Programming Model for an Embedded Media Processing Architecture"  
*Dan Zhang (Xi'an Jiaotong University, China), Zeng-Zhi Li (Xi'an Jiaotong University, China), Hong Song (Xi'an Shiyong University, China), and Long Liu (Xi'an Jiaotong University, China)*
- 12:50 "RAPANUI: Rapid Prototyping for Media Processor Architecture Exploration"  
*Guillermo Payá Vayá, Javier Martín Langerwerf, and Peter Pirsch (University of Hannover, Germany)*

## Wednesday, July 20

### Architectures and Implementations

*Session chair: Dirk Stroobandt*

- 8:30 "A Radix-8 Multiplier Design and Its Extension for Efficient Implementation of Imaging Algorithms"  
*David Guevorkian (Nokia, Finland), Petri Liuha (Nokia, Finland), Aki Launiainen (Nokia, Finland), Konsta Punkka (Tampere Univ. Tech., Finland), and Ville Lappalainen (Nokia, Finland)*
- 8:50 "FPL-3E: Towards Language Support for Reconfigurable Packet Processing"  
*Mihai Lucian Cristea (Leiden University, The Netherlands), Claudiu Zissulescu (Leiden University, The Netherlands), Ed Deprettere (Leiden University, The Netherlands), and Herbert Bos (Vrije Universiteit Amsterdam, The Netherlands)*
- 9:10 "A Routing Paradigm with Novel Resources Estimation and Routability Models for X-Architecture Based Physical Design"  
*Yu Hu (Tsinghua University, China), Tong Jing (Tsinghua University, China), Xianlong Hong (Tsinghua University, China), Xiaodong Hu (Chinese Academy of Sciences, China), and Guiying Yan (Chinese Academy of Sciences, China)*
- 9:30 "Benchmarking Mesh and Hierarchical Bus Networks in System-on-Chip Context"  
*Erno Salminen (Tampere Univ. Tech. Finland), Tero Kangas (Tampere Univ. Tech. Finland), Jouni Riihimäki (Nokia, Finland), Vesa Lahtinen (Nokia, Finland), Kimmo Kuusilinna (Nokia, Finland), and Timo D. Hämmäläinen (Tampere Univ. Tech. Finland)*
- 9:50 **Posters**
- "A Case for Visualization-Integrated System-Level Design Space Exploration"  
*Andy D. Pimentel (University of Amsterdam, The Netherlands)*

"Mixed Virtual/Real Prototypes for Incremental System Design -A Proof of Concept"  
*Stefan Eilers and C. Müller-Schloer (University Hannover, Germany)*

## **System Level Design, Modeling, and Simulation**

*Session chair: David Gevorkian*

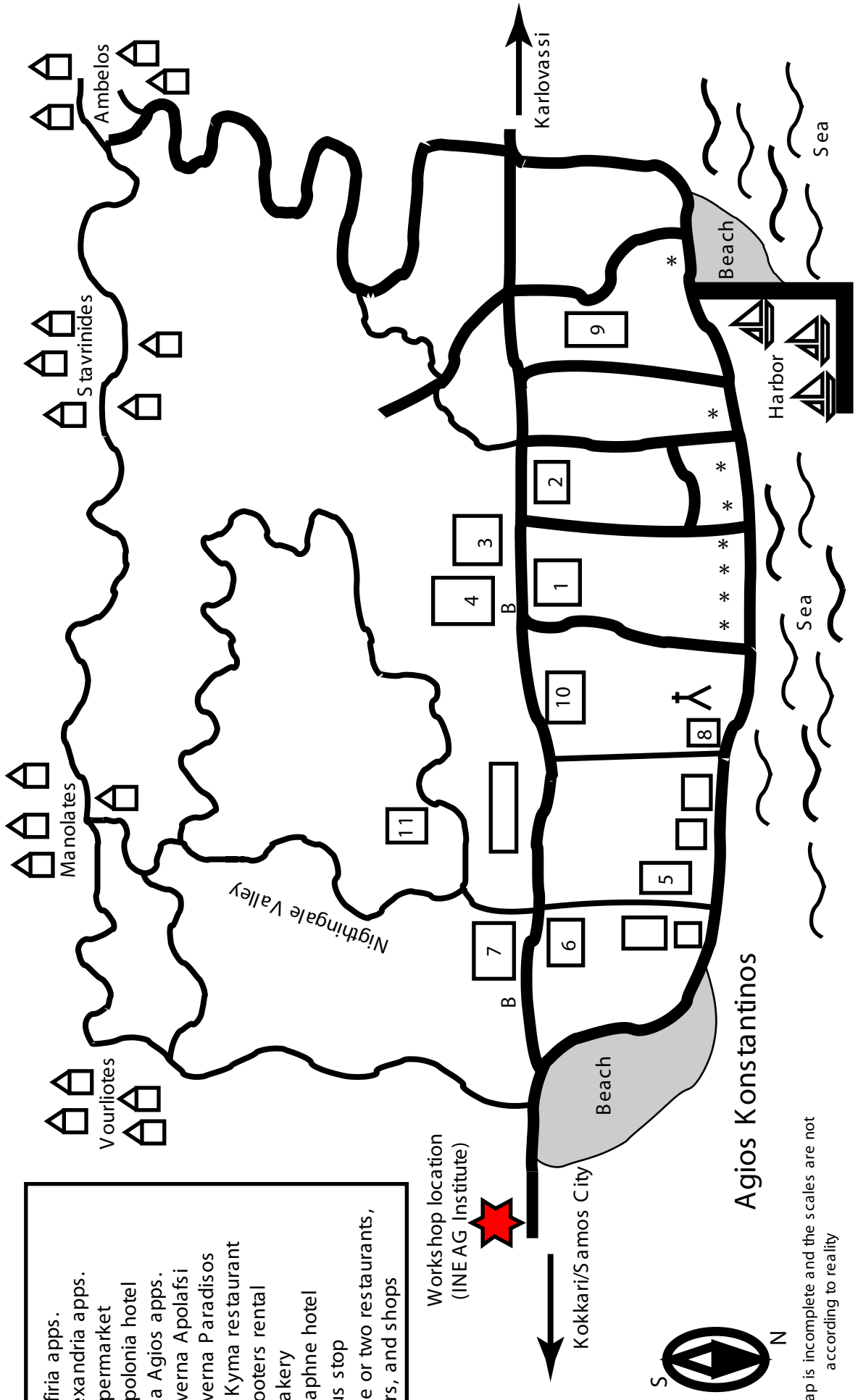
- 10:10 "Modeling NoC Architectures by Means of Deterministic and Stochastic Petri Nets"  
*H. Blume, T. von Sydow, D. Becker, and T.G. Noll (RWTH Aachen University, Germany)*
- 10:30 "High Abstraction Level Design and Implementation Framework for Wireless Sensor Networks"  
*Mauri Kuorilehto, Mikko Kohvakka, Marko Hännikäinen, and Timo D. Hämmäläinen (Tampere Univ. Tech., Finland)*
- 10:50 "The ODYSSEY Tool-Set for System-Level Synthesis of Object-Oriented Models"  
*Maziar Goudarzi and Shaahin Hessabi (Sharif University of Technology, Iran)*
- 11:10 "Design and Implementation of a WLAN Terminal Using UML 2.0 Based Design Flow"  
*Petri Kukkala, Marko Hännikäinen, and Timo D. Hämmäläinen (Tampere Univ. Tech., Finland)*

## **11:30 Demonstrations**

*Session chair: Timo Hämmäläinen*

- 11:50 "Rapid Implementation and Optimisation of DSP Systems on SoPC Heterogeneous Platforms"  
*J. McAllister, R. Woods, D. Reilly, S. Fischaber, and R. Hasson (Queens University Belfast, UK)*
- 12:10 "DVB-DSNG Modem High Level Synthesis in an Optimized Latency Insensitive System Context"  
*P. Bomel (UBS University, France), N. Abdelli (THALES, France), E. Martin (UBS University, France), A.-M. Fouilliant, E. Boutillon (UBS University, France), and P. Kajfasz (THALES, France)*
- 12:30 "SystemQ: A Queuing-Based Approach to Architecture Performance Evaluation with SystemC"  
*Sören Sonntag, Matthias Gries, and Christian Sauer (Infineon, Germany)*
- 12:50 "Moving Up to the Modeling Level for the Transformation of Data Structures in Embedded Multimedia Applications"  
*Marijn Temmerman (Karel de Grote-Hogeschool, Belgium), Edgar G. Daylight (IMEC, Belgium), Francky Catthoor (IMEC, Belgium), Serge Demeyer (Universiteit Antwerpen, Belgium), and Tom Dhaene (Universiteit Antwerpen, Belgium)*
- 13:10 **Closing**  
*Stamatis Vassiliadis (Delft University of Technology, The Netherlands)*

- 1 - Zafiria apps.
- 2 - Alexandria apps.
- 3 - Supermarket
- 4 - Appolonia hotel
- 5 - Villa Agios apps.
- 6 - Taverna Apolafsi
- 7 - Taverna Paradisos
- 8 - To Kyma restaurant
- 9 - Scooters rental
- 10 - Bakery
- 11 - Daphne hotel
- B - Bus stop
- \* - One or two restaurants, bars, and shops



This map is incomplete and the scales are not according to reality