



SAMOS VI:
Embedded Computer Systems:
Architectures, MOdeling, and Simulation
 July 17-20 2006, Samos, Greece

International Conference SAMOS VI

Room A

Monday, 17 July	
8:30	Opening
	<i>Jarmo Takala, Tampere Univ. Tech.</i>
Keynote	
8:45	Reconfigurable Platform for Digital Convergence Terminals
	<i>Jinsung Chi (Senior Vice President and Head of Mobile Communication Technology, Research Lab LG Electronics)</i>
9:25	Coffee break (20 Min)
Embedded Processors and Architectures	
	Session Chair: <i>Mladen Berekovic, IMEC</i>
9:45	Parallel Memory Implementation for Arbitrary Stride Accesses
	<i>Eero Aho, Jarmo Vanne, Timo Hämäläinen (Institute of Digital and Computer Systems, Tampere University of Technology)</i>
10:10	A Table-Based Application-Specific Prefetch Engine for Object-Oriented Embedded Systems
	<i>Mehdi Modarressi, Maziar Goudarzi, Shaahin Hessabi, Hani JavanHemmat (Sharif university of technology, Tehran, Iran)</i>

International Workshop SAMOS VI

Room B

Monday, 17 July	
Opening and Keynote are common to Workshop and Conference Participants	
9:25	Coffee break (20 Min)
System Design and Modeling I	
	Session Chair: <i>Timo D. Hämäläinen, Tampere Univ. Tech.</i>
9:45	Interface overheads in embedded multimedia software
	<i>Tero Rintaluoma (Hantro Products Oy, Oulu, Finland), Olli Silven (Department of Electrical and Information Engineering, University of Oulu, Finland), and Juuso Raekallio (Hantro Products Oy, Oulu, Finland)</i>
10:10	A UML profile for Asynchronous Hardware Design
	<i>Kim Sandström and Ian Oliver (Nokia Research Center, Finland)</i>

International Workshop SAMOS VI

Room C

Monday, 17 July	
Opening and Keynote are common to Workshop and Conference Participants	
9:25	Coffee break (20 Min)
Wireless Sensor Networks	
	Session Chair: <i>Marko Hännikäinen, Tampere Univ. Tech.</i>
9:45	Designing Wireless Sensor Nodes
	<i>Marcos A. M. Vieira, Adriano B. da Cunha, and Di'ogenes C. da Silva Jr. (Federal University of Minas Gerais, Brazil)</i>
10:10	Design, Implementation, and Experiments on Outdoor Deployment of Wireless Sensor Network for Environmental Monitoring
	<i>Jukka Suhonen, Mikko Kohvakka, Marko Hännikäinen, and Timo D. Hämäläinen (Tampere University of Technology, Institute of Computer and Digital Systems, Finland)</i>

10:35	On the Characterization of Data Cache Vulnerability in High-Performance Embedded Microprocessors
	<i>Shuai Wang, Jie Hu, Sotirios Ziarvas (Dept. of Electrical and Computer Engineering, New Jersey Institute of Technology)</i>
11:00	On the Evaluation of Dense Chip-Multiprocessor Architectures
	<i>Francisco J. Villa Aroca, Manuel E. Acacio Sanchez, Jose M. Garcia Carrasco (University of Murcia)</i>
11:25	Coffee break (20 Min)
Energy Aware Processors	
	Session Chair: <i>Daniel Iancu, Sandbrige Technologies</i>
11:45	Reduction of Energy Consumption in Processors by Early Detection and Bypassing of Trivial Operations
	<i>Md. Mafijul Islam (BRAC University), Per Stenstrom (Chalmers University of Technology)</i>
12:10	Modified Hot-Spot Cache Architecture
	<i>Kashif Ali, Mokhtar Aboelaze, Suprakash Datta (York University)</i>
12:35	Static Energy Saving Through Multi-Bank Memory Architecture
	<i>Sebastien Lafond (Turku Centre for Computer Science), Johan Lilius (Abo Akademy University)</i>

10:35	Key research challenges for successfully applying MDD within RTES development
	<i>Aram Hovsepian, Stefan Van Baelen, Bert Vanhooff, Wouter Joosen, and Yolande Berbers (Department of Computer Science, Katholieke Universiteit Leuven, Belgium)</i>
11:00	Towards a Transformation Chain Modeling Language
	<i>Bert Vanhooff, Stefan Van Baelen, Aram Hovsepian, Wouter Joosen, and Yolande Berbers (Department of Computer Science, Katholieke Universiteit Leuven, Belgium)</i>
11:25	Coffee break (20 Min)
System Design and Modeling I continued	
	Session Chair: <i>Timo D. Hämmäläinen, Tampere Univ. Tech.</i>
11:45	An Optimization Methodology for Memory Allocation and Task Scheduling in SoCs via Linear Programming
	<i>Bastian Ristau and Gerhard Fettweis (TU Dresden, Vodafone Chair Mobile Communications Systems, Germany)</i>
12:10	Efficient Automated Clock Gating Using CoDeL
	<i>Nainesh Agarwal and Nikitas J. Dimopoulos (Department of Electrical and Computer Engineering, University of Victoria, Canada)</i>

10:35	LATONA: An Advanced Server Architecture for Ubiquitous Sensor Network
	<i>Chi-Hoon Shin (University of Science and Technology, Rep. of Korea), Soo-Cheol Oh, Dae-Won Kim, Sun-Wook Kim, Kyoung Park, and Sung-Woon Kim (Server Platform Research Team, Electronics and Telecommunications Research Institute, Rep. of Korea)</i>
11:00	An Approach for Reduction of Power Consumption in Sensor Nodes of Wireless Sensor Networks: Case Analysis of Mica2
	<i>Adriano B. da Cunha, and Di'ogenes C. da Silva Jr. (Dept. of Electrical Engineering, Federal University of Minas Gerais, Brazil)</i>
11:25	Coffee break (20 Min)
Wireless Sensor Networks continued	
	Session Chair: <i>Marko Hämmäläinen, Tampere Univ. Tech.</i>
11:45	Energy-driven partitioning of signal processing algorithms in sensor networks
	<i>Dong-Ik Ko, Chung-Ching Shen, Shuvra S. Bhattacharyya, and Neil Goldsman (University of Maryland, USA)</i>
12:10	Preamble Sense Multiple Access (PSMA) for Impulse Radio-Ultra Wideband Sensor Networks
	<i>Jussi Haapola, Leonardo Goratti, Isameldin Suliman, and Alberto Rabbachin (Centre for Wireless Communications (CWC), University of Oulu, Finland)</i>
12:35	Security in Wireless Sensor Networks: Considerations and Experiments
	<i>Panu Hämmäläinen, Mauri Kuorilehto, Timo Alho, Marko Hämmäläinen, and Timo D. Hämmäläinen (Tampere University of Technology, Institute of Digital and Computer Systems, Finland)</i>

13:00	Area-Aware Performance and Power Optimizations for Resource Constrained Embedded Processors
	<i>Amirali Baniyadi (University of Victoria), Babak Salamat (University of California, Irvine), Kaveh Jokar Deris (University of Victoria)</i>

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Room A

Tuesday, 18 July	
Keynote EU	
	Session Chair: <i>Stamatis Vassiliadis, Tech. Univ. Delft</i>
8:30	European research in embedded systems
	<i>Panagiotis Tsarchopoulos, (Embedded Systems Unit, European Commission)</i>
9:10	Coffee break (20 Min)
Design Space Exploration I	
	Session Chair: <i>Shuvra Bhattacharyya, Univ. Maryland</i>
9:30	Chip Size Estimation for SOC Design Space Exploration
	<i>Hartwig Jeschke (Institut fuer Mikroelektronische Systeme)</i>
9:55	Profiling Driven Scenario Detection and Prediction for Multimedia Applications
	<i>Stefan Valentin Gheorghita, Twan Basten, Henk Corporaal (Eindhoven University of Technology)</i>
10:20	On the Calibration of Abstract Performance Models for System-level Design Space Exploration
	<i>Andy Pimentel, Mark Thompson, Simon Polstra, Cagkan Erbas (University of Amsterdam)</i>

Room B

Tuesday, 18 July	
Keynote is common to Workshop and Conference Participants	
9:10	Coffee break (20 Min)
System Design and Modeling II	
	Session Chair: <i>Nikitas Dimopoulos, Univ. Victoria</i>
9:30	Automated Distribution of UML 2.0 Designed Applications to a Configurable Multiprocessor Platform
	<i>Mikko Setälä, Petri Kukkala, Tero Arpinen, Marko Hännikäinen, and Timo D. Hämäläinen (Tampere University of Technology, Institute of Digital and Computer Systems, Finland)</i>
9:55	Domain-specific Modeling of Power Aware Distributed Real-time Embedded Systems
	<i>Gabor Madl and Nikil Dutt (Center for Embedded Computer Systems, University of California, Irvine, USA)</i>
10:20	Mining Dynamic Document Spaces with Massively Parallel Embedded Processors
	<i>Jan W. M. Jacobs (Océ Technologies BV, The Netherlands), Rui Dai (National University of Singapore, Design Technology Institute Faculty of Engineering, Singapore), and Gerard J.M. Smit (University of Twente, The Netherlands)</i>

Room C

Tuesday, 18 July	
Keynote is common to Workshop and Conference Participants	
9:10	Coffee break (20 Min)
Processor Design I	
	Session Chair: <i>Olli Silvén, Univ. Oulu</i>
9:30	Effects of Program Compression
	<i>Jari Heikkinen and Jarmo Takala (Tampere University of Technology, Finland)</i>
9:55	Energy Optimization of a Multi-banks Main Memory
	<i>Hanene Ben Fradj, Sébastien Icart, Cécile Belleudy, and Michel Auguin (Laboratoire d'informatique, Signaux et Systèmes de Sophia-Antipolis, France)</i>
10:20	Probabilistic Modelling and Evaluation of Soft Real-Time Embedded Systems
	<i>Oana Florescu (Eindhoven University of Technology), Menno de Hoon (Chess Information Technology BV), Jeroen Voeten (Eindhoven University of Technology), and Henk Corporaal (Eindhoven University of Technology)</i>

10:45	Pareto-based application specification for MP-SoC customized run-time management
	<i>Chantal Ykman-Couvreur, Vincent Nollet, Theo Marescaux, Erik Brockmeyer, Francky Catthoor (IMEC), Henk Corporaal (Technical University Eindhoven)</i>
11:10 Coffee break (20 Min)	
Design Space Exploration II	
	Session Chair: <i>Andy Pimentel, Univ. Amsterdam</i>
11:30	Performance Improvements in Microprocessor Systems Utilizing a Coprocessor Data-Path
	<i>Michalis Galanis, Gregory Dimitroulakos, Costas Goutis (University of Patras)</i>
11:55	Multi-Objective Topology Optimization for Networked Embedded Systems
	<i>Thilo Streichert, Christian Haubelt, Jurgen Teich (University of Erlangen-Nuremberg)</i>
12:20	Parameterized Mapping of Algorithms onto Processor Array with Sub-Word Parallelism
	<i>Rainer Schaffer, Renate Merker (Institute of Circuits and Systems, Dresden University of Technology)</i>
12:45	Hardware DWT accelerator for MultiProcessor System On-Chip on FPGA
	<i>Simone Borgio, Davide Bosisio, Fabrizio Ferrandi, Marco D. Santambrogio, Donatella Sciuto, Antonino Tumeo (Politecnico di Milano)</i>

11:10 Coffee break (20 Min)	
Dependable Computing	
	Session Chair: <i>Stefanos Kaxiras, Univ. Patras</i>
11:30	CARROT – A Tool for Fast and Accurate Soft Error Rate Estimation
	<i>Dimitrios Bountas and Georgios I. Stamoulis (Department of Computer and Communications Engineering, University of Thessaly, Greece)</i>
11:55	A Scheduling Strategy for a Real-Time Dependable Organic Middleware
	<i>Uwe Brinkschulte, Alexander von Renteln, and Mathias Pacher (Institute for Process Control and Robotics, University of Karlsruhe)</i>
12:20	Autonomous Construction Technology of Community for Achieving High Assurance Service
	<i>Kotaro Hama, Yuji Horikoshi, Yosuke Sugiyama, and Kinji Mori (Department of Computer Science, Tokyo Institute of Technology, Japan)</i>
12:45	Preventing Denial-of-Service Attacks in Shared CMP Caches
	<i>Georgios Keramidas, Pavlos Petoumenos, Stefanos Kaxiras, Alexandros (Department of Electrical and Computer Engineering, University of Patras, Greece)</i>

10:45	Hybrid Functional and Instruction Level Power Modeling for Embedded Processors
	<i>Holger Blume (RWTH Aachen University), Daniel Becker (RWTH Aachen University), Martin Botteck (Nokia Research Center), Jörg Brakensiek (Nokia Research Center), and Tobias G. Noll (RWTH Aachen University)</i>
11:10 Coffee break (20 Min)	
Processor Design II	
	Session Chair: <i>Georgi N. Gaydadjiev, Tech. Univ. Delft</i>
11:30	Software Pipelining Support for Transport Triggered Architecture Processors
	<i>Perttu Salmela (Tampere University of Technology), Pekka Jääskeläinen (Tampere University of Technology), Tuomas Järvinen (Nokia Technology Platforms), and Jarmo Takala (Tampere University of Technology)</i>
11:55	Low-Power, High-Performance TTA Processor for 1024 Point Fast Fourier Transform
	<i>Teemu Pitkänen, Risto Mäkinen, Jari Heikkinen, Tero Partanen, and Jarmo Takala (Tampere University of Technology, Finland)</i>
12:20	A Scalable, Multi-Thread, Multi-Issue Array Processor Architecture for DSP Applications Based on Extended Tomasulo Scheme
	<i>Mladen Berekovic (IMEC, Belgium, and TU Delft, The Netherlands) and Tim Niggemeier (IBM Deutschland Entwicklung GmbH, Germany)</i>
12:45	Code Size Reduction by Compiler Tuning
	<i>Masayo Haneda, Peter M. W. Knijnenburg, and Harry A.G. Wijshoff (LIACS, Leiden University, The Netherlands)</i>

Room A

Wednesday, 19 July	
High Level System Design and Simulation	
	Session Chair: <i>Ed Deprettere, Univ. Leiden</i>
8:30	An Efficient Hierarchical Fuzzy Approach for System Level System-on-a-Chip Design
	<i>Giuseppe Ascia, Vincenzo Catania, Alessandro Di Nuovo, Maurizio Palesi, Davide Patti (Dipartimento di Ingegneria Informatica e delle Telecomunicazioni, Universita di Catania)</i>
8:55	Accelerating RTL Simulation by Several Orders of Magnitude Using Clock Suppression
	<i>Hannes Muhr (Vienna University of Technology, Institute of Computer Technology), Roland Holler (Vienna University of Applied Sciences, Technikum Wien)</i>
9:20	SimGate: Full-System, Cycle-Close Simulation of the Stargate Sensor Network Intermediate Node
	<i>Ye Wen, Selim Gurun, Navraj Chohan, Rich Wolski, Chandra Krintz (University of California, Santa Barbara)</i>
9:45	Memory-constrained Block Processing Optimization for Synthesis of DSP Software
	<i>Ming-Yung Ko, Chung-Ching Shen, Shuvra Bhattacharyya (Dept. of Electrical and Computer Engineering, University of Maryland)</i>

Room B

Wednesday, 19 July	
Architectures and Implementations I	
	Session Chair: <i>John Glossner, Sandbrige Technologies</i>
8:55	Design of Asynchronous Embedded Processor with New Ternary Data Encoding Scheme
	<i>Je-Hoon Lee, Eun-Ju Choi, and Kyoung-Rok Cho (Dept. of Computer and Communication Eng., Chungbuk National University, Rep. of Korea)</i>
9:20	Hardware-based IP lookup using n-way set associative memory and LPM comparator
	<i>SangKyun Yun (Department of Computer and Telecommunications Engineering, Yonsei University, Rep. of Korea)</i>
Architectures and Implementations II	
	Session Chair: <i>Fabrizio Ferrandi, (Politecnico di Milano)</i>
9:45	A Flash File System to Support Fast Mounting for NAND Flash Memory Based Embedded Systems
	<i>Song-Hwa Park, Tae-Hoon Lee, and Ki-Dong Chung (Pusan National University, Rep. of Korea)</i>

Room C

Wednesday, 19 July	
Processor Design III	
	Session Chair: <i>Luigi Carro, Univ. Rio Grande do Sul</i>
8:30	Integrated Instruction Scheduling and Fine-Grain Register Allocation for Embedded Processors
	<i>Dae-Hwan Kim and Hyuk-Jae Lee (School of Electrical Engineering and Computer Science, Seoul National University, Rep. of Korea)</i>
8:55	Compilation and Simulation Tool Chain for Memory Aware Energy Optimizations
	<i>Manish Verma, Lars Wehmeyer, Robert Pyka, Peter Marwedel (Department of Computer Science XII, University of Dortmund, Germany), and Luca Benini (DEIS, University of Bologna, Italy)</i>
9:20	MPEG4 encoder prefetching using Flux Caches
	<i>Georgi N. Gaydadjiev and Stamatis Vassiliadis (TU Delft, The Netherlands)</i>
9:45	Reducing Execution Unit Leakage Power in Embedded Processors
	<i>Houman Homayoun and Amirali Baniasadi (Electrical and Computer Engineering Department, University of Victoria, Canada)</i>

10:10	Coffee break (20 Min)
System and NoC Platforms	
	Session Chair: <i>Jürgen Teich, Univ. Erlangen-Nürnberg</i>
10:30	Exploration of Distributed Shared Memory Architectures for NoC-based Multiprocessors
	<i>Cristina Silvano, Matteo Monchiero, Gianluca Palermo, Oreste Villa (Politecnico di Milano)</i>
10:55	Performance Evaluation of RISC-based SoC Platforms in Network Processing Applications
	<i>Rainer Ohlendorf, Thomas Wild, Michael Meitinger, Holm Rauchfuss, Andreas Herkersdorf (Munich University of Technology)</i>
11:20	FLUX Networks: Interconnects on Demand
	<i>Stamatis Vassiliadis, Ioannis Sourdis (EEMCS, TU Delft, The Netherlands)</i>
11:45	Coffee break (20 Min)
Reconfigurable Processors and Applications of ES	
	Session Chair: <i>Stefan Wong, Tech. Univ. Delft</i>
12:05	On-Chip Communication in Run-Time Assembled Reconfigurable Systems
	<i>Pete Sedcole, Peter Cheung, George Constantinides, Wayne Luk (Imperial College London)</i>

10:10	Coffee break (20 Min)
10:30	Rescheduling for Optimized SHA-1 Calculation
	<i>Ricardo Chaves, Georgi Kuzmanov, Leonel Sousa, and Stamatis Vassiliadis (TU Delft, The Netherlands)</i>
10:55	Software Implementation of WiMAX on the Sandbridge SandBlaster Platform
	<i>Daniel Iancu, Hua Ye, Emanoil Surducan, Murugappan Senthilvelan, John Glossner, Vasile Surducan, Vladimir Kotlyar, Andrei Iancu, Gary Nacer, and Jarmo Takala (Sandbridge Technologies, USA)</i>
Architectures and Implementations III	
	Session Chair: <i>Jarmo Takala, Tampere Univ. Tech.</i>
11:20	High-Radix Addition and Multiplication in the Electron Counting Paradigm using Single Electron Tunneling Technology
	<i>Cor Meenderinck and Sorin Cotofana (TU Delft, The Netherlands)</i>
11:45	Coffee break (20 Min)
12:05	Area, Delay, and Power Characteristics of Standard-Cell Implementations of the AES S-Box
	<i>Stefan Tillich, Martin Feldhofer, and Johann Großschädl (Graz University of Technology, Institute for Applied Information Processing and Communications, Austria)</i>

10:10	Coffee break (20 Min)
Processor Design IV	
	Session Chair: <i>Holger Blume, RWTH Aachen University</i>
10:30	Memory architecture evaluation for video encoding on enhanced embedded processors
	<i>Ali Iranpour and Krzysztof Kuchcinski (Lund University, Department of Computer Science, Sweden)</i>
10:55	Advantages of Java Processors in Cache Performance and Power for Embedded Applications
	<i>Antonio Carlos S. Beck, Mateus B. Rutzig, and Luigi Carro (Instituto de Informática, Universidade Federal do Rio Grande do Sul, Brazil)</i>
Embedded Sensor Systems	
	Session Chair: <i>Georgi N. Gaydadjiev, Tech. Univ. Delft</i>
11:20	Integrated Microsystems in Industrial Applications
	<i>Paddy J. French (Ei/EWI-DIMES, TU Delft, The Netherlands)</i>
11:45	Coffee break (20 Min)
12:05	A Solid-State 2-D Wind Sensor
	<i>Kofi A.A. Makinwa, Johan H. Huijsing, Arend Hagedoorn (Ei/EWI-DIMES, TU Delft, The Netherlands)</i>

12:30	Multi-objective Optimal Controller Synthesis for Heterogeneous Embedded Systems
	<i>Lech Jozwiak, Dominik Gawlowski, Aleksander Slusarczyk (Eindhoven University of Technology)</i>
12:55	Throughput optimization via cache partitioning for embedded multiprocessors
	<i>Anca Molnos, Sorin Cotofana (T.U. Delft), Marc Heijligers, Jos van Eijndhoven (Philips Research)</i>
13:20	Closing
	<i>Stamatis Vassiliadis (EEMCS, TU Delft, The Netherlands)</i>

Thursday, 20 July	
8:30	Hiking
	<i>Stamatis Vassiliadis (EEMCS, TU Delft, The Netherlands)</i>

12:30	A Method for Router Table Compression for Application Specific Routing in Mesh Topology NoC Architectures
	<i>Maurizio Palesi (DIIT, University of Catania, Italy), Shashi Kumar (Jönköping University, Sweden), and Rickard Holsmark (Jönköping University, Sweden)</i>
Closing is common to Workshop and Conference Participants	

Thursday, 20 July	
Hiking is common to Workshop and Conference Participants	

12:30	Fault-Tolerant Bus System for Airbag Sensors and Actuators
	<i>Klaas-Jan de Langen (Philips Semiconductors, Nijmegen, The Netherlands)</i>
12:55	Principal Component Analysis and Artificial Neural Network Based Approach to Analysing Optical Fibre Sensors Signals
	<i>E. Lewis, C. Sheridan, M. O'Farrell, D.J. King, C. Flanagan, W. Lyons and C. Fitzpatrick (University of Limerick, Ireland)</i>
Closing is common to Workshop and Conference Participants	

Thursday, 20 July	
Hiking is common to Workshop and Conference Participants	