



SAMOS VII:
Embedded Computer Systems:
Architectures, MOdeling, and Simulation
 July 16-19 2007, Samos, Greece

Conference

Workshop

Track 2

Monday

Track 1

Monday

Monday

08:30 Opening Opening and Keynote are common to Workshop and Conference Participants
Session Chairs: Holger Blume, RWTH Aachen University; Mladen Berekovic, IMEC-NL
08:45 Keynote 1: Willie Anderson, VP Engineering for Qualcomm CDMA Technologies

09:25 Coffee Break (20 min)

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09:25 Coffee Break (20 min)

Session 1 Processor Architectures
Session Chair: Holger Blume, RWTH Aachen University

09:45 IC-Presentation 1
Applying Data Mapping Techniques to Vector DSPs

 Peter Westermann (University of Dortmund, Germany),
 Ludwig Schwoerer and Andre Kaufmann (Nokia Research
 Center Bochum, Germany)

10:10 IC-Presentation 2
**Instruction Set Encoding Optimization for Code Size
 Reduction**
 Michael Med and Andreas Krall (Technical University
 Vienna, Austria)

10:35 IC-Presentation 3
**FlexCore: Utilizing Exposed Datapath Control for
 Efficient Computing**

 Martin Thuresson, Magnus Sjalander, Magnus Björk,
 Lars Svensson, Per Larsson-Edefors and Per Stenstrom
 (Chalmers University of Technology, Sweden)

11:00 IC-Presentation 4
**Prototyping Efficient Interprocessor Communication
 Mechanisms**

 Vassilis Papaefstathiou, Dionisios Pnevmatikatos,
 Manolis Marazakis, Giorgos Kalokairinos, Aggelos
 Ioannou,
 Michael Papamichael, Stamatias Kavadias, Giorgos
 Mihelogiannakis and Manolis Katevenis (Institute of
 Computer Science, FORTH, Heraklion, Greece)

11:25 Coffee Break (20 min)

Session 1 System Modeling and Simulation
Session Chair: Andy Pimentel, Univ. of Amsterdam

09:45 WS-Presentation 1
**Communication Architecture Simulation
 on the Virtual Synchronization Framework**
 Taewook Oh, Youngmin Yi, Soonhoi Ha (School of
 EECS, Seoul National University, Korea)

10:10 WS-Presentation 2
**A Model-Driven Automatically-Retargetable
 Debug Tool for Embedded Systems**
 Max R. de O. Schultz, Alexandre K. I. Mendonça,
 Felipe G. Carvalho, Olinto J. V. Furtado, Luiz C. V.
 Santos (UFSC:Federal University of Santa
 Catarina, Brazil)

10:35 WS-Presentation 3
**Performance Evaluation of Memory
 Management Configurations in Linux for an OS-
 Level Design Space Exploration**
 Sangsoo Park (University of Michigan, USA) and
 Heonshik Shin (Seoul National University, Korea)

11:00 WS-Presentation 4
**SC2SCFL: Automated SystemC to SystemCFL
 Translation**

 Ka Lok Man (UCC, Cork, Ireland.), Andrea Fedeli
 (STMicroelectronics, Milan, Italy), Michele Mercaldi
 (M.O.S.T., Turin, Italy), Menouer Boubekeur (UCC,
 Cork, Ireland.), Michel Schellekens (UCC, Cork,
 Ireland.)

11:25 Coffee Break (20 min)

Session 1 VLSI Architectures
Session Chair: Mladen Berekovic, IMEC-NL

09:45 WS-Presentation 27
**Model and Validation of Block Cleaning
 Cost for Flash Memory**
 Seungjae Baek, Jongmoo Choi, (Dankook University,
 Korea) Donghee Lee (University of Seoul, Korea) and
 Sam H. Noh (Hongik University, Korea)

10:10 WS-Presentation 28
**VLSI Architecture for MRF based Stereo
 Matching**
 Sungchan Park, Chao Chen, Hong Jeong (Pohang
 University of Science and Technology, Korea)

10:35 WS-Presentation 29
**Low-Power Twiddle Factor Unit for FFT
 Computation**

 Teemu Pitkanen, Tero Partanen and Jarmo Takala
 (Tampere University of Technology, Finland)

11:00 WS-Presentation 30
**Trade-offs Between Voltage Scaling and
 Processor Shutdown for Low-Energy Embedded
 Multiprocessors**

 Pepijn De Langen, Ben Juurlink (Delft University of
 Technology, Netherlands)

11:25 Coffee Break (20 min)

| Session 2 Design Space Exploration | |
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| Session Chair: <i>Stephan Wong, Tech. University Delft</i> | |
| 11:45 IC-Presentation 5 | Design Space Exploration of Configuration Manager for Network Processing Application |
| Christoforos Kachris and Stamatis Vassiliadis (Delft University of Technology, Netherlands) | |
| 12:10 IC-Presentation 6 | Design Space Exploration of Media Processors: A Parameterized Scheduler |
| Guillermo Payá-Vayá, Javier Martín-Langerwerf, Piriya Taptimthong and Peter Pirsch (University of Hannover, Germany) | |
| 12:35 IC-Presentation 7 | Automatic bus matrix synthesis based on hardware interface selection for fast communication design space exploration |
| Ganghee Lee, Seokhyun Lee, Youngjin Ahn and Kiyoung Choi (Seoul National University, Korea) | |
| 13:00 IC-Presentation 8 | Systematic Data Structure Exploration of Multimedia and Network Applications realized Embedded Systems |
| Lazaros Papadopoulos, Christos Baloukas, Nikolaos Zompakis and Dimitrios Soudris (Democritus University Thrace, Xanthi, Greece) | |

End of the presentation sessions: 13:25

Tuesday

08:20 Introduction Keynote is common to Workshop and Conference Participants
 Session Chair: *Jarmo Takala, Tampere Univ. Tech.*
 08:30 Keynote 2: **Jos Huiskens, Silicon Hive "Integrating VLIW processors with a network on chip"**

09:10 Coffee Break (20 min)

| Session 3 Multiprocessor Architectures | |
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| Session Chair: <i>Georgi Gaydadjiev, Tech. University Delft</i> | |
| 09:30 IC-Presentation 9 | On the Problem of Minimizing Workload Execution Time in SMT Processors |
| Francisco J Cazorla (Barcelona Supercomputing Center, Spain), Peter M.W. Knijnenburg (University of Amsterdam, Netherlands), Rizos Sakellariou (University of Manchester, U.K.), Enrique Fernandez (Universidad de Las Palmas de Gran Canaria, Spain.), Alex Ramirez and Mateo Valero (Universitat Politècnica de Catalunya, Spain) | |

| Session 2 Scheduling & Programming Models | |
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| Session Chair: <i>Martin Botteck, Nokia Research Bochum</i> | |
| 11:45 WS-Presentation 5 | An Automatically-Retargetable Time-Constraint-Driven Instruction Scheduler for Post-Compiling Optimization of Embedded Code |
| José Otávio Carlomagno Filho, Luiz Fernando Penkal Santos, Luiz Claudio Villar dos Santos (Federal University of Santa Catarina, Brazil) | |
| 12:10 WS-Presentation 6 | Improving TriMedia cache performance by profile guided code reordering |
| Norbert Esser (NXP Semiconductors, US), Renga Sundararajan (NXP Semiconductors, US), and Joachim Trescher (NXP Research, Netherlands) | |
| 12:35 WS-Presentation 7 | A streaming machine description and programming model |
| Paul Carpenter, David Rodenas, Xavier Carpenter, Alex Ramirez, Eduard Ayguade (UPC, Spain) | |
| 13:00 WS-Presentation 8 | An Approach of SWFG-based Code Selection in Sequential Image Processing Algorithms |
| Dan Wu, Zhiying Wang, Shaogan Wang (National University of Defense Technology, PR China) | |

End of the presentation sessions: 13:25

Tuesday

09:10 Coffee Break (20 min)

| Session 3 Reconfigurable Architectures | |
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| Session Chair: <i>Oli Silven, Univ. of Oulu</i> | |
| 09:30 WS-Presentation 9 | MORA: A New Coarse-Grain Reconfigurable Array for High Throughput Multimedia Processing |
| Marco Lanuzza, Stefania Perri and Pasquale Corsonello (Dept. of Electronics - University of Calabria - Italy) | |

| Session 2 Multi-Processor Architectures | |
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| Session Chair: <i>Jarmo Takala, Tampere Univ. Tech.</i> | |
| 11:45 WS-Presentation 31 | Mapping and Performance Evaluation for heterogeneous MP-SoCs via Packing |
| Bastian Ristau and Gerhard Fettweis (TU Dresden, Vodafone Chair Mobile Communications Syst, Germany) | |
| 12:10 WS-Presentation 32 | Strategies for Compiling μTC to Novel Chip Multiprocessors |
| Thomas A.M. Bernard, Chris R. Jesshope, Peter M.W. Knijnenburg (CSA, Informatics Institute, University of Amsterdam, Netherlands) | |
| 12:35 WS-Presentation 33 | Image Quantisation on a Massively Parallel Embedded Processor |
| Jan Jacobs, Leroy van Engelen, Jan Kuper, Gerard J.M. Smit (University of Twente, Netherlands) | |
| 13:00 WS-Presentation 34 | Stream Image Processing on a Dual-Core Embedded System |
| Michael Benjamin and David Kaeli (Northeastern University, US) | |

End of the WS-Presentation sessions: 13:25

Tuesday

09:10 Coffee Break (20 min)

| Session 3 Design Space Exploration | |
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| Session Chair: <i>Koen Bertels, Tech. University Delft</i> | |
| 09:30 WS-Presentation 35 | Efficiency Measures for Multimedia SOCs |
| Hartwig Jeschke (Institute of Microelectronic Systems, University of Hannover, Germany) | |

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| <p>09:55 IC-Presentation 10 Performance and Power Analysis of Parallelized Implementations on an MPCore Multiprocessor Platform Holger Blume, Jörg von Livonius, Lisa Rotenberg (RWTH Aachen University, Germany), Harald Bothe, Joerg Brakensiek (Nokia Research Center Bochum, Germany) and Tobias G. Noll (RWTH Aachen University, Germany)</p> |
| <p>10:20 IC-Presentation 11 An Interrupt Controller for FPGA-based Multiprocessors Antonino Tumeo, Marco Branca, Lorenzo Camerini, Matteo Monchiero, Gianluca Palermo, Fabrizio Ferrandi and Donatella Sciuto (Politecnico di Milano, Italy)</p> |
| <p>10:45 IC-Presentation 12 Application Case Studies on HS-Scale, a MP-SOC for Embedded Systems Nicolas Saint-Jean, Pascal Benoit, Gilles Sassatelli, Lionel Torres and Michel Robert (University of Montpellier, France)</p> |

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| <p>09:55 WS-Presentation 10 FPGA design Methodology for a Wavelet-Based Scalable Video Decoder Hendrik Eeckhout, Harald Devos, Philippe Faes, Mark Christiaens, Dirk Stroobandt (Ghent University, Belgium)</p> |
| <p>10:20 WS-Presentation 11 Evaluating Large System-on-Chip on Multi-FPGA Platform Arii Kulmala, Erno Salminen, Timo D. Hämäläinen (Tampere University of Technology, Finland)</p> |

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| <p>09:55 WS-Presentation 36 On-chip Bus modeling for Power and Performance Estimation Je-Hoon Lee, (Chungbuk Nat'l Univ. BK21 Chungbuk Information Technology Center, Korea) Young-Shin Cho (Samsung SDI), Seok-Man Kim, Kyoung-Rok Cho (Chungbuk Nat'l Univ., Korea)</p> |
| <p>10:20 WS-Presentation 37 A Framework Introducing Model Reversibility in SoC Design Space Exploration Alexis van der Biest Alienor Richard, Dragomir Mилоjevic, Frederic Robert (Université Libre de Bruxelles, Belgium)</p> |
| <p>10:45 WS-Presentation 38 Towards Multi-application Workload Modeling in Sesame for System-level Design Space Exploration Mark Thompson, Andy D. Pimentel (University of Amsterdam, Netherlands)</p> |

11:10 Coffee Break (20 min)

11:10 Coffee Break (20 min)

11:10 Coffee Break (20 min)

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| <p>Session 4 Systems and Applications Session Chair: Martin Botteck, Nokia Research Bochum</p> |
| <p>11:30 IC-Presentation 13 A Hardware/Software Architecture for Tool Path Computation. An Application to Turning Lathe Machining Sergio Cuenca, Antonio Martinez, Antonio Jimeno and Jose Luis Sanchez (University of Alicante, Spain)</p> |
| <p>11:55 IC-Presentation 14 Energy efficiency of mobile video decoding Tero Rintaluoma (Hantro Products Oy, Oulu, Finland) and Olli Silvén (University of Oulu, Finland)</p> |
| <p>12:20 IC-Presentation 15 Instruction-Level Fault Tolerance Configurability Demid Borodin, Ben Juurlink and Stamatis Vassiliadis (Delft University of Technology, Netherlands)</p> |
| <p>12:45 IC-Presentation 16 The Weight-Watcher Service and its Lightweight Implementation Benoît Garbinato (Université de Lausanne, Switzerland), Rachid Guerraoui, Jarle Hulaas, Alexei Kounine, Maxime Monod and Jesper Spring (Ecole Polytechnique Federale de Lausanne, Switzerland)</p> |

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| <p>Session 4 Processor Components Session Chair: Nikitas Dimopoulos, Univ. Victoria</p> |
| <p>11:30 WS-Presentation 12 Resource Conflict Detection in Simulation of Function Unit Pipelines Pekka Jääskeläinen, Vladimír Guzma, Jarmo Takala (Tampere University of Technology, Finland)</p> |
| <p>11:55 WS-Presentation 13 A Modular Coprocessor Architecture for Embedded Real-Time Image and Video Signal Processing Holger Flatt, Sebastian Hesselbarth, Sebastian Fluegel and Peter Pirsch (Institute of Microelectronic Systems, University of Hannover, Germany)</p> |
| <p>12:20 WS-Presentation 14 High-bandwidth Address Generation Unit Humberto Calderon, Carlo Galuzzi, Georgi Gaydadjiev, Stamatis Vassiliadis (TU Delft, Netherlands)</p> |
| <p>12:45 WS-Presentation 15 An IP Core for Embedded Java Systems Sascha Uhrig, Jörg Mische and Theo Ungerer (University of Augsburg, Germany)</p> |

End of the presentation sessions: 13:10

End of the presentation sessions: 13:10

Wednesday**Session 5 Reconfigurable Architectures***Session Chair: John McAllister, Queen's Univ. Belfast*

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| 08:30 IC-Presentation 17 | COSMOS: A System-Level Modelling and Simulation Framework for Coprocessor-Coupled Reconfigurable Systems Kehuai Wu and Jan Madsen (Technical University of Denmark) |
| 08:45 IC-Presentation 18 | Flexibility Inlining into Custom Arithmetic Data-paths Exploiting A Regular Interconnection Scheme Sotiris Xydis, George Economakos and Kiamal Pekmestzi (National Technical University of Athens Greece) |
| 09:20 IC-Presentation 19 | An Evolutionary Approach to Area-Time Optimization of FPGA designs Fabrizio Ferrandi, Pier Luca Lanzi, Gianluca Palermo, Christian Pilato, Donatella Sciuto and Antonino Tumeo (Politecnico di Milano, Italy) |
| 09:45 IC-Presentation 20 | The ARISE Reconfigurable Instruction Set Extensions Framework Nikolaos Vassiliadis, George Theodoridis and Spiridon Nikolaidis (Aristotle University of Thessaloniki) |

10:10 Coffee Break (20 min)

Session 6 Memory Architectures and Memory Optimization*Session Chair: Andy Pimentel, Univ. of Amsterdam*

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| 10:30 IC-Presentation 21 | Simulative Buffer Analysis of Local Image Processing Algorithms Described by Windowed Synchronous Data Flow Joachim Keinert (Fraunhofer IIS Erlangen, Germany), Christian Haubelt and Jürgen Teich (University of Erlangen-Nuremberg, Germany) |
| 10:55 IC-Presentation 22 | Online Prediction of Applications Cache Utility Miquel Moretó (Universitat Politècnica de Catalunya, Barcelona, Spain), Francisco J. Cazorla, Alex Ramirez and Mateo Valero (Barcelona Supercomputing Center, Spain) |

Wednesday**Session 5 Embedded Processors***Session Chair: Hartwig Jeschke, Univ. of Hannover*

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| 08:30 WS-Presentation 16 | Parallel Memory Architecture for TTA Processor Jarno Tanskanen, Teemu Pitkänen, Risto Mäkinen (Plenware Oy, Finland), and Jarmo Takala (Tampere University of Technology, Finland) |
| 08:55 WS-Presentation 17 | A Linear Complexity Algorithm for the Generation of Multiple Input Single Output Instructions of Variable Size Carlo Galuzzi, Koen Bertels and Stamatis Vassiliadis (TU Delft, Netherlands) |
| 09:20 WS-Presentation 18 | Automated Power Gating of Registers using CoDeL and FSM Branch Prediction Nainesh Agarwal, Nikitas Dimopoulos (University of Victoria, Canada) |
| 09:45 WS-Presentation 19 | A Study of Energy Saving in Customizable Processors Paolo Bonzini, Dilek Harmanci, Laura Pozzi (University of Lugano, Switzerland) |

10:10 Coffee Break (20 min)

Session 6 SoC for SDR (I)*Session Chair: Bruno Bougard, IMEC*

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| 10:30 WS-Presentation 20 | Trends in Low Power Handset Software Defined Radio John Glossner, Daniel Iancu, Mayan Moudgill (Sandbridge, USA), Michael Schulte (University of Wisconsin, USA) and Stamatis Vassiliadis (TU Delft, Netherlands) |
| 10:55 WS-Presentation 21 | Design of a Low Power Pre-Synchronization ASIP for Multimode SDR Terminals Thomas Schuster, Bruno Bougard, Praveen Raghavan, Robert Prieuwater, David Novo, Liesbet Van der Perre, Francky Cathoor (IMEC, Belgium) |

Wednesday**Session 5 EU-Session***Session Chair: Georgij Kuzmanov, Tech. University Delft*

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| 08:30 Part A: Computer Architectures | Project SARC , Georgi Gaydadjiev, TU Delft Project SHAPES , Alberto dell'Olio, Atmel Roma Project AETHER , Jean-Marc Philippe, CEA-LIST |
| 09:00 Part B: Addaptive Technologies | Project 4S , Ralf Koenig, Univ. Karlsruhe Project hArtes , Roberto Marega, Atmel Roma Project MORPHEUS , Koen Bertels, TU Delft |
| 09:30 Part C: Brainstorming Discussions | |

10:10 Coffee Break (20 min)

Session 6 Wireless Sensors (I)*Session Chair: Oli Silven, Univ. of Oulu*

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| 10:30 WS-Presentation 43 | Design of 100 μW Wireless Sensor Nodes on Energy Scavengers for Biomedical Monitoring Lennart Ysebodt (Eindhoven University of Technology), Michael De Nil (Eindhoven University of Technology), Jos Huisken, (SiliconHive) Mladen Berekovic (IMEC), Qin Zhao (IMEC), Frank Bouwens (IMEC) and Jef van Meerbergen (Philips Research) - all Netherlands |
| 10:55 WS-Presentation 44 | Tool-Aided Design and Implementation of Indoor Surveillance Wireless Sensor Network Mauri Kuorilehto, Jukka Suhonen, Marko Hännikäinen, Timo D. Hämaläinen (Tampere University of Technology, Finland) |

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| <p>11:20 IC-Presentation 23 Maximum and sorted cache occupation using array padding</p> <p>Ezequiel Herruzo (University of Cordoba, Spain), Emilio L. Zapata and Oscar Plata (University of Malaga, Spain)</p> |
| <p>11:45 IC-Presentation 24 A Memory-Efficient Reconfigurable Aho-Corasick FSM Implementation for Intrusion Detection Systems</p> <p>Vassilis Dimopoulos, Ioannis Papaefstathiou and Dionysis Pnevmatikatos (Technical University of Crete, Chania, Greece)</p> |

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| <p>11:20 WS-Presentation 22 Area efficient fully programmable baseband processors</p> <p>Anders Nilsson and Dake Liu (Linkoping University, Sweden)</p> |
| <p>11:45 WS-Presentation 23 The Next Generation Challenge for Software Defined Radio</p> <p>Mark Who, Sangwon Seo, Hyunseok Lee, Yuan Lin, Scott Mahlke, Trevor Mudge (all University of Michigan Ann Arbor, USA), Chaitali Chakrabarti (Arizona State University, USA) and Krisztian Flautner (ARM Ltd. UK)</p> |

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| <p>11:20 WS-Presentation 45 System Architecture Modeling of an UWB Receiver for Wireless Sensor Network</p> <p>Aubin Lecointre, Daniela Dragomirescu, Robert Planas (LAAS-CNRS, Toulouse, France)</p> |
| <p>11:45 WS-Presentation 46 An embedded Platform with Duty-cycled Radio and Processing Subsystems for Wireless Sensor Networks</p> <p>Zhong-Yi Jin, Curt Schurgers, Rajesh Gupta (UCSD, Ca-USA)</p> |

12:10 Coffee Break (20 min) 12:10 Coffee Break (20 min) 12:10 Coffee Break (20 min)

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| <p>Session 7 Cryptography <i>Session Chair: Nikitas Dimopoulos, Univ. Victoria</i></p> |
| <p>12:30 IC-Presentation 25 A side-channel attack resistant programmable PKC coprocessor for embedded applications</p> <p>Nele Mentens, Kazuo Sakiyama, Lejla Batina, Bart Preneel and Ingrid Verbauwhede (KU Leuven, Belgium)</p> |
| <p>12:55 IC-Presentation 26 Secure and Authenticated Communication in Chip-Level Microcomputer Bus Systems with Tree Parity Machines</p> <p>Sascha Muehlbach and Sebastian Wallner (Hamburg University of Technology, Germany)</p> |
| <p>13:20 IC-Presentation 27 A Simulation-Based Methodology for Evaluating the DPA-Resistance of Cryptographic Functional Units with Application to CMOS and MCML Technologies</p> <p>Francesco Regazzoni (University of Lugano, Switzerland), Stéphane Badel (EPFL, Switzerland), Thomas Eisenbarth (Ruhr-University of Bochum, Germany), Johann Großschädl (University of Bristol, U.K.), Axel Poschmann (Ruhr-University of Bochum, Germany), Zeynep Toprak (EPFL, Switzerland), Marco Macchetti (C.E. Consulting, Milan, Italy), Laura Pozzi (University of Lugano, Switzerland), Christof Paar (Ruhr-University of Bochum, Germany), Yusuf Leblebici and Paolo Ienne (EPFL, Switzerland)</p> |

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| <p>Session 7 SoC for SDR (II) <i>Session Chair: John Glossner, Sandbridge</i></p> |
| <p>12:30 WS-Presentation 24 Design Methodology for Software Radio Systems</p> <p>Chia-han Lee, Wayne Wolf (Princeton University, USA)</p> |
| <p>12:55 WS-Presentation 25 Power Efficient Co-Simulation Framework for a Wireless Application Using Platform Based SoC</p> <p>Tseesuren Batsuuri, Je-Hoon Lee, Kyoung-Rok Cho (Chungbuk Nat'l University, Korea)</p> |
| <p>13:20 WS-Presentation 26 A Comparative Study of Different FFT Architectures for Software Defined Radio</p> <p>Shashank Mittal, Md. Zafar Ali Khan, M.B. Srinivas (IIIT Hyderabad, India)</p> |

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| <p>Session 7 Wireless Sensors (II) <i>Session Chair: Stephan Wong, Tech. University Delft</i></p> |
| <p>12:30 WS-Presentation 47 SensorOS: a New Operating System for Time Critical WSN Applications</p> <p>Mauri Kuorilehto, Timo Alho (Nokia Technology Platforms, Finland), Marko Hännikäinen, Timo D. Hämäläinen (Tampere University of Technology, Finland)</p> |
| <p>12:55 WS-Presentation 48 Review of Hardware Architectures for Advanced Encryption Standard Implementations Considering Wireless Sensor Networks</p> <p>Pamu Hämäläinen (Nokia Technology Platforms, Finland), Marko Hännikäinen, Timo D. Hämäläinen (Tampere University of Technology, Finland)</p> |
| <p>13:20 WS-Presentation 49 k+ Neigh: An Energy Efficient Topology Control for Wireless Sensor Networks</p> <p>Dong-Min Son, Young-Bae Ko (Ajou University, Korea)</p> |

End of the presentation sessions: 13:45

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13:45 Closing Remarks Closing is common to Workshop and Conference Participants
Session Chair: Georgi Gaydadjev, Tech. University Delft

End of Conference: 14:00