

# Schedule for the Samos Symposium 2008 (21-24 July 2008)

| Conference   |  | Conference   |  | Workshop   |  |
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| Track 1  |  | Track 2  |  | Track 1  |  |
| Monday - 21 July 2008  |  | Monday - 21 July 2008  |  | Monday - 21 July 2008  |  |
| 08:30 Opening<br><i>Session Chair: Jarmo Takala</i>  |  | 08:30 Opening<br><i>Session Chair: Jarmo Takala</i>  |  | 08:30 Opening<br><i>Session Chair: Jarmo Takala</i>  |  |
| 09:00 Keynote: "PicoServer - Building a Compact Energy Efficient Multiprocessor"<br><i>Trevor Mudge, University of Michigan</i>  |  | 09:00 Keynote: "PicoServer - Building a Compact Energy Efficient Multiprocessor"<br><i>Trevor Mudge, University of Michigan</i>  |  | 09:00 Keynote: "PicoServer - Building a Compact Energy Efficient Multiprocessor"<br><i>Trevor Mudge, University of Michigan</i>  |  |
| 09:40 Coffee Break (20 min)  |  | 09:40 Coffee Break (20 min)  |  | 09:40 Coffee Break (20 min)  |  |
| <b>Session IC1.1 EMBEDDED PARALLEL SYSTEMS</b><br><i>Session Chair: Georgi Gaydadjiev</i>  |  | <b>Session IC2.1 DESIGN SPACE EXPLORATION</b><br><i>Session Chair: Jarmo Takala</i>  |  | <b>Session WS1.1 ARCHITECTURE</b><br><i>Session Chair: John Glossner</i>   |  |
| 10:00 A General Model of Concurrency and its Implementation as Many-core Dynamic RISC Processors<br><i>T. Bernard, K. Bousias, L. Guang, C. R. Jesshope, M. Lankamp, M. W. van Tol, and L. Zhang</i> |  | 10:00 Systematic Design Space Exploration for Customisable Multi-Processor Architectures<br><i>Ben Cope, Peter Y.K. Cheung, and Wayne Luk</i>  |  | 10:00 On the Benefit of Caching Traffic Flow Data in the Link Buffer<br><i>Konstantin Septinus, Christian Grimm, Vladislav Rummyantsev, and Peter Pirsch</i>   |  |
| 10:25 A Parameterized Dataflow Language Extension for Embedded Streaming Systems<br><i>Yuan Lin, Yoonseo Choi, Scott Mahlke, Trevor Mudge, and Chaitali Chakrabarti</i>                              |  | 10:25 A Clustering Method for the Identification of Convex Disconnected Multiple Input Multiple Output Instructions<br><i>Carlo Galuzzi, Dimitri Theodoropoulos, and Koehn Bertels</i> |  | 10:25 Energy-efficient Simultaneous Thread Fetch from Different Cache Levels in a Soft Real-time SMT Processor<br><i>Emre Özer, Ronald G. Dreslinski, Trevor Mudge, Stuart Biles, and Krisztián Flautner</i> |  |
| 10:50 An Architecture for the Simultaneous Execution of Hard Real-Time Threads<br><i>Jonathan Barre, Christine Rochange, and Pascal Sainrat</i>  |  | 10:50 Multi-Objective Routing and Topology Optimization in Networked Embedded Systems<br><i>Michael Glass, Martin Lukasiewicz, Rolf Wanka, Christian Haubelt, and Jürgen Teich</i>     |  | 10:50 Impact of Software Bypassing on Instruction Level Parallelism and Register File Traffic<br><i>Vladimir Guzma, Pekka Jääskeläinen, Pertti Kellomäki, and Jarmo Takala</i>                               |  |
| 11:15 An Adaptive Bloom Filter Cache Partitioning Scheme for Multicore Architectures<br><i>Konstantinos Nikas, Matthew Horsnell, and Jim Garside</i>   |  | 11:15 Scalable Architecture for Prefix Preserving Anonymization of IP Addresses<br><i>Anthony Blake and Richard Nelson</i>   |  |  |  |
| 11:40 Coffee Break (20 min)  |  | 11:40 Coffee Break (20 min)  |  | 11:40 Coffee Break (20 min)  |  |
| <b>Session IC1.2 NETWORK ON A CHIP</b><br><i>Session Chair: Trevor Mudge</i>   |  | <b>Session IC2.2 APPLICATIONS</b><br><i>Session Chair: Alex Veidenbaum</i>   |  | <b>Session WS1.2 NEW FRONTIERS</b><br><i>Session Chair: Andy Pimentel</i>  |  |
| 12:00 On Brain-inspired Hybrid Topologies for Nano-architectures – A Rent's Rule Approach –<br><i>Valeriu Beiu, Basheer A. M. Madappuram, and Martin McGinnity</i>                                   |  | 12:00 ImpBench - A Novel Benchmark Suite for Biomedical, Microelectronic Implants<br><i>Christos Strydis, Christoforos Kachris, and Georgi N. Gaydadjiev</i>                           |  | 12:00 Arithmetic Design on Quantum-Dot Cellular Automata Nanotechnology<br><i>Ismo Hänninen and Jarmo Takala</i>   |  |
| 12:25 Realizing Reconfigurable Mesh Algorithms on Softcore Arrays<br><i>Heiner Giefers and Marco Platzner</i>  |  | 12:25 Perceptual Feature based Music Classification - A DSP Perspective for a New Type of Application<br><i>H. Blume, M. Haller, M. Botteck, and W. Theimer</i>                        |  | 12:25 Preliminary Analysis of the Cell BE Processor Limitations for Sequence Alignment Applications<br><i>Sebastian Isaza, Friman Sanchez, Georgi Gaydadjiev, Alex Ramirez, and Mateo Valero</i>             |  |
| 12:50 A Light-Weight Network-on-Chip Architecture for Dynamically Reconfigurable Systems<br><i>Simone Corbetta, Vincenzo Rana, Marco Domenico Santambrogio, and Donatella Sciuto</i>                 |  | 12:50 Software Defined Radio Implementation of K-best List Sphere Detector Algorithm<br><i>Janne Janhunen, Olli Silvén, Markku Juntti, and Markus Myllylä</i>                          |  | 12:50 802.15.3 Transmitter: A fast design cycle using OFDM framework in Bluespec<br><i>Teemu Pitkänen, Vesa-Matti Hartikainen, Nirav Dave, and Gopal Raghavan</i>  |  |
| End of the presentation sessions: 13:15  |  | End of the presentation sessions: 13:15  |  | End of the presentation sessions: 13:15  |  |
| BEACH NOTE: "Can they be fixed? Some thoughts after 40 years in the business" (during social event)<br><i>Yale Patt, University of Texas-Austin</i>  |  |  |  |  |  |

| Conference   |  | Workshop   |  | Workshop  |  |
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| Track 1  |  | Track 1  |  | Track 2   |  |
| Tuesday - 22 July 2008   |  | Tuesday - 22 July 2008   |  | Tuesday - 22 July 2008  |  |
| 08:20 Introduction<br><i>Session Chair: John Glossner</i>  |  |  |  |   |  |
| 08:30 Keynote: "Challenges in Embedded System Simulation"<br><i>Tor Jeremiassen, Texas Instruments</i>   |  |  |  |   |  |
| 09:10 Coffee Break (20 min)  |  | 09:10 Coffee Break (20 min)  |  | 09:10 Coffee Break (20 min)   |  |
| <b>Session IC1.3 PROCESSOR ARCHITECTURE</b>  |  | <b>Session WS1.3 SoC</b>   |  | <b>Session WS2.3 Special Session: SYSTEM LEVEL DESIGN FOR HETEROGENEOUS SYSTEMS</b>   |  |
| <i>Session Chair: Cristina Silvano</i>   |  | <i>Session Chair: Mladen Berekovic</i>   |  | <i>Session Chair: John McAllister</i>   |  |
| 09:30 Fine-grained Application-specific Instruction Set Processor Design for the K-best List Sphere<br><b>Detector Algorithm</b><br><i>Juho Antikainen, Perttu Salmela, Olli Silvén, Markku Juntti, Jarmo Takala, and Markus Myllylä</i>       |  | 09:30 A Real-Time Programming Model for Heterogeneous MPSoCs<br><i>Torsten Limberg, Bastian Ristau, and Gerhard Fettweis</i>   |  | 09:30 Streaming Systems in FPGAs<br><i>Stephen Neuendorffer and Kees Vissers</i>  |  |
| 09:55 An Instruction Set Extension for Java Bytecodes Translation Acceleration<br><i>Isidoros Sideris, Kiamal Pekmezci, and George Economakos</i>  |  | 09:55 A Multi-Objective and Hierarchical Exploration Tool for SoC Performance Estimation<br><i>Alexis Vander Blest, Alienor Richard, Dragomir Milojevic, and Frederic Robert</i> |  | 09:55 Heterogeneous Design in Functional DIF<br><i>William Plishker, Nimish Sane, Mary Kiemb, and Shuvra S. Bhattacharyya</i>   |  |
| 10:20 Architectural and Algorithm level Fault Tolerant Techniques for Low Power High Yield Multimedia Devices<br><i>Mohammad A. Makhzan (Avesta Sasan), Ahmed Eltawil, and Fadi J. Kurdahi</i>   |  | 10:20 A Novel Non-Exclusive Dual-Mode Architecture for MPSoCs-Oriented Network on Chip Designs<br><i>Francesca Palumbo, Simone Secchi, Danilo Pani, and Luigi Raffo</i>          |  | 10:20 Tool Integration and Interoperability Challenges of a System-level Design Flow: a Case Study<br><i>Andy D. Pimentel, Todor Stefanov, Hristo Nikolov, Mark Thompson, Simon Polstra, and Ed F. Deprettere</i> |  |
| 10:45 Comparative Architectural Characterization of SPEC CPU2000 and CPU2006 Benchmarks on the Intel Core 2 Duo Processor<br><i>Arun Kejariwal, Alexander V. Veidenbaum, Alexandru Nicolau, Xinmin Tian, Milind Girkar, and Utpal Banerjee</i> |  | 10:45 Energy and Performance Evaluation of an FPGA-based SoC Platform with AES and PRESENT Coprocessors<br><i>Xu Guo, Zhimin Chen, and Patrick Schaumont</i>                     |  | 10:45 Evaluation of ASIPs Design with LISATek<br><i>Rashid Muhammad, Ludovic Aprville and Renaud Pacalet</i>  |  |
| 11:10 Coffee Break (20 min)  |  | 11:10 Coffee Break (20 min)  |  | 11:10 Coffee Break (20 min)   |  |
| <b>Session IC1.4 MULTIPROCESSORS</b>   |  | <b>Session WS1.4 APPLICATION SPECIFIC DESIGNS</b>  |  | <b>Session WS2.4 Special Session: SYSTEM LEVEL DESIGN FOR HETEROGENEOUS SYSTEMS</b>   |  |
| <i>Session Chair: Koen Bertels</i>   |  | <i>Session Chair: Yale Patt</i>  |  | <i>Session Chair: John McAllister</i>   |  |
| 11:30 Ant Colony Optimization for Mapping and Scheduling in Heterogeneous Multiprocessor Systems<br><i>Antonino Tumeo, Christian Pilato, Fabrizio Ferrandi, Donatella Sciuto, and Pier Luca Lanzi</i>  |  | 11:30 Area Reliability trade-off in Improved Reed Muller Coding<br><i>Costas Argyrides, Stephanía Loizidou, and Dhiraj K. Pradhan</i>  |  | 11:30 High Level Loop Transformation for Systematic Signal Processing Embedded Applications<br><i>Calin Glitia and Pierre Boulet</i>  |  |
| 11:55 An Efficient Design Space Exploration Methodology for Multiprocessor SoC Architectures based on Response Surface Methods<br><i>Gianluca Palermo, Cristina Silvano, and Vittorio Zaccaria</i>   |  | 11:55 Efficient Reed-Solomon Iterative Decoder Using Galois Field Instruction Set<br><i>Daniel Iancu, Mayan Moudgill, John Glossner, and Jarmo Takala</i>                        |  | 11:55 Memory-Centric Hardware Synthesis from Dataflow Models<br><i>Scott Fischhaber, John McAllister, and Roger Woods</i>   |  |
| 12:20 Efficient Management of Speculative Data in Hardware Transactional Memory Systems<br><i>M. M. Waliullah and Per Stenstrom</i>  |  | 12:20 ASIP-eFPGA Architecture for Multioperable GNSS Receivers<br><i>Thorsten von Sydow, Holger Blume, Götz Kappen, and Tobias G. Noll</i>                                       |  | <b>Session WS2.6 SYSTEM MODELING AND DESIGN</b>   |  |
| 12:45 An Intermediate Format for Automatic Generation of MPSoC Virtual Prototypes<br><i>Alexandre Chureau and Frédéric Pétrot</i>  |  | <b>Session WS2.6 SYSTEM MODELING AND DESIGN</b>  |  | 12:20 Signature-based Calibration of Analytical System-level Performance Models<br><i>Stanley Jaddoe and Andy D. Pimentel</i>   |  |
|  |  | 12:45 Intellectual Property Protection for Embedded Sensor Nodes<br><i>Michael Gora, Patrick Schaumont, and Eric Simpson</i>   |  | 12:45 System Level Design Space Exploration of Dynamic Reconfigurable Architectures<br><i>Kamana Sigdel, Mark Thompson, Andy D. Pimentel, Todor Stefanov, and Koen Bertels</i>                                    |  |
| End of the presentation sessions: 13:10  |  | End of the presentation sessions: 13:10  |  | End of the presentation sessions: 13:10   |  |

| Conference   | Workshop   | Workshop   |
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| Track 1<br>Wednesday - 23 July 2008  | Track 1<br>Wednesday - 23 July 2008  | Track 2<br>Wednesday - 23 July 2008  |
| <p>08:20 Introduction<br/> <i>Session Chair: Georgi Gaydadjiev</i><br/>           08:30 Keynote: "Towards Unified IPC Mechanisms"<br/> <i>Manolis Katevenis, University of Crete</i></p> |  |  |
| 09:10 Coffee Break (15 min)  |  |  |
| <b>Session IC1.5 RECONFIGURABLE COMPUTING</b>  | <b>Session WS1.5 Special Session: PROGRAMMING MULTICORES</b>   | <b>Session WS2.5 SENSORS AND SENSOR NETWORKS</b>   |
| <i>Session Chair: Jean-Luc Gaudiot</i>   | <i>Session Chair: Chris Jesshope</i>   | <i>Session Chair: Dragomir Milocevic</i>   |
| 09:25 Exploiting Partial Reconfiguration for Flexible Software Debugging<br><i>Giovanni Busonera, Alessandro Forin, and Richard Neil Pittman</i>   | 09:25 Deterministic Parallel Programming in SVP<br><i>Chris Jesshope</i>   | 09:25 Climate and Biological Sensor Network<br><i>Perfecto Mariño, Fernando Pérez Fontán, Miguel Ángel Domínguez, and Santiago Otero</i>   |
| 09:50 A Cost Model for Partial Dynamic Reconfiguration<br><i>Markus Rullmann and Renate Merker</i>   | 09:50 A Quest for Performance Portability in the Many-core Era<br><i>Albert Cohen</i>  | 09:50 Monitoring of Environmentally Hazardous Exhaust Emissions from Cars using Optical Fibre Sensors<br><i>Elfed Lewis, John Clifford, Colin Fitzpatrick, Gerard Dooly, Weizhong Zhao, Tong Sun, Ken Grattan, James Lucas, Martin Degner, Hartmut Ewald, Steffen Lochmann, Gero Bramann, Edoardo Merlone-Borla, and Flavio Gili</i> |
| 10:15 Reconfigurable Design with Clock Gating<br><i>W.G. Osborne, W. Luk, J. G. F. Coutinho, and O. Mencer</i>   | 10:15 Stream Processing with S-Net<br><i>Clemens Greck</i>   | 10:15 Application Server for Wireless Sensor Networks<br><i>Janne Rintanen, Jukka Suhonen, Marko Hännikäinen, and Timo D. Hämäläinen</i>   |
| 10:40 Reconfigurable Design with Clock Gating<br><i>W.G. Osborne, W. Luk, J. G. F. Coutinho, and O. Mencer</i>   | 10:40 Programming Multi-core Systems Using a Declarative Model of Concurrency<br><i>Farhad Arbab</i>   | 10:40 Embedded Software Architecture for Diagnosing Network and Node Failures in Wireless Sensor Networks<br><i>Jukka Suhonen, Mikko Kohvakka, Marko Hännikäinen, and Timo D. Hämäläinen</i>   |
| 11:05 Coffee Break (15 min)  |  |  |
| <b>Session IC1.6 MEMORY AND CACHES</b>   | <b>Session WS1.6 Special Session: PROGRAMMING MULTICORES</b>   | <b>EU Session HARTES BRAINSTORMING SESSION</b>   |
| <i>Session Chair: Olli Silvén</i>  | <i>Session Chair: Chris Jesshope</i>   | <i>Session Chair: Koen Bertels</i>   |
| 11:20 A Centralized Cache Miss Driven Technique to Improve Processor Power Dissipation<br><i>Houman Homayoun, Mohammad Makhzan, Jean-Luc Gaudiot, and Alex Veidenbaum</i>                | 11:20 Design Issues in Parallel Array Languages for Shared Memory<br><i>James Brodman, Basilio B. Fraguela, María J. Garzaran, and David Padua</i>   | 11:20 HARTES BRAINSTORMING   |
| 11:45 A Priority-Expression-Based Burst Scheduling of Memory Reordering Access<br><i>Jun Pang, Lei Yang, Lei Shi, Tiejun Zhang, Donghui Wang, and Chaohuan Hou</i>                       | 11:45 Array Programming: Anachronism or Unrecognized Gem?<br><i>Sven-Bodo Scholz</i>   | 11:45 HARTES BRAINSTORMING   |
| 12:10 Improving Memory Subsystem Performance in Network Processors with Smart Packet Segmentation<br><i>Kimon Karras, Daniel Llorente, Thomas Wild, and Andreas Herkersdorf</i>          | 12:10 An Architecture and Protocol for the Management of Resources in Ubiquitous and Heterogeneous Systems based on the SVP model of Concurrency<br><i>Chris Jesshope, Jean-Marc Philippe, and Michiel van Tol</i> | 12:10 HARTES BRAINSTORMING   |
| 12:35 Improving TLB Energy for Java Applications on JVM<br><i>Chinnakrishnan S. Ballapuram and Hsien-Hsin S. Lee</i>   |  | 12:35 HARTES BRAINSTORMING   |
| 13:00 Coffee Break (5 min)   |  |  |
| 13:05 Closing Remarks  |  |  |

End of Conference: 13:30